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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/611,948	07/03/2003	Hisashi Ishikawa	00862.023127.	5415

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EXAMINER	
VO, QUANG N	
ART UNIT	PAPER NUMBER
2625	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/611,948	ISHIKAWA, HISASHI	
	Examiner	Art Unit	
	Quang N. Vo	2625	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 February 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-7,20,22-26 and 39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-7,20,22-26 and 39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 02/24/09 has been entered.

Response to Arguments

Applicant's arguments with respect to claims have been considered but are moot in view of the new ground(s) of rejection.

Regarding claim 1, Applicant's argument is Katayama does not disclose or suggest i) a quantization component that receives an integral portion (upper bits) of corrected image data, and quantizes the received integer portion of the corrected image data, ii) an inverse quantizing component that inverse-quantizes the quantized integer portion of the corrected image data, and outputs an inverse-quantized data, iii) a calculation component that outputs a quantization error based on a difference between the integer portion of the corrected image data and the inverse-quantized data, iv) a buffer that stores the calculated quantization error, and v) an error diffusion component that generates a correction value to be added to input data of a next pixel by diffusing the quantization error stored in said buffer.

In response: Katayama discloses a quantization component (e.g., binarizing means block 903, figure 25) that receives an integral portion (upper bits) of the

corrected image data and quantizes the received integer portion of the corrected image data (e.g., binarizing means 903 for binarizing a signal output from the data adding means 902, figure 25, column 19, lines 47-49); a buffer that stores the calculated quantization error (e.g., error distributing means 907 and block 908, figure 25) and an error diffusion component (e.g., error storing means block 908 and data adding means block 902, figures 25) that generates a correction value to be added to input data of a next pixel by diffusing the quantization error stored in said buffer (e.g., data adding means (block 902) for adding an input image signal to an error distributed from neighboring pixels, figure 25, column 19, lines 40-65).

Katayama does not explicitly disclose an inverse quantizing component that inverse-quantizes the quantized integer portion of the corrected image data, and outputs an inverse-quantized data; a calculation component that outputs a quantization error based on a difference between the integer portion of the corrected image data and the inverse-quantized data.

Ishikawa's 075 discloses an inverse quantizing component (e.g., inverse quantizer 31, figure 3) that inverse-quantizes the quantized integer portion of the corrected image data (e.g., output from quantizer 13 (integer portion), figure 3), and outputs an inverse-quantized data (e.g., the quantized representative values of the CMY signals outputted by the inverse quantizer 31, column 8, lines 19-21); a calculation component (e.g., The adder/subtractor 32, column 8, line 18) that outputs a quantization error based on a difference between the integer portion of the corrected image data (e.g., subtracting the CMY signals outputted by the offset adder 17, column 8, lines 18-

19) and the inverse-quantized data (e.g., the quantized representative values of the CMY signals outputted by the inverse quantizer 31, column 8, lines 19-21).

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to have modified Katayama to include an inverse quantizing component that inverse-quantizes the quantized integer portion of the corrected image data, and outputs an inverse-quantized data; a calculation component that outputs a quantization error based on a difference between the integer portion of the corrected image data and the inverse-quantized data as taught by Ishikawa's 075. It would have been obvious to one of ordinary skill in the art at the time of the invention to have modified Katayama by the teaching of Ishikawa to conveniently diffuse error to neighboring pixels to have better image quality.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 3, 7, 20, 22, 26, and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Katayama et al. (Katayama) (US 5,488,673) in view of Ishikawa (US 6,330,075).

With regard to claim 1, Katayama discloses an image processing apparatus (e.g., an image processing apparatus, figure 26) comprising: a bit connection component (e.g., a program storing in the ROM 912 for executing adding pixel data to error data (a

bit connection), block S3, figure 28, column 20, lines 4-6) that connects a decimal portion of image data (e.g., a distribution-error value (decimal portion), column 20, lines 36-37) of a preceding pixel (e.g., objective pixel, column 20, lines 44-46) output from a latch component (e.g., error storing means block 908, figure 25), to image data of a target pixel as lower bits of the image data of the target pixel (e.g., a neighboring pixel (a target pixel), column 20, lines 44-48), and outputs the bit-connected image data having an integer portion (e.g., binarizing means block 903 (integer portion), figure 25) of the image data of the target pixel and the decimal portion (e.g., a distribution-error value (decimal portion), figure 25); a correction component (e.g., data adding means block 902, error-to-be-distributed computing means block 903, and error storing means block 908, figure 25) that generates corrected image data by adding a correction value to the bit-connected image data (e.g., data adding means 902 for adding an input image signal to an error distributed from neighboring pixels, column 19, lines 44-47), the corrected image data having the integer portion (e.g., error-to-be-distributed computing means 904 for performing integral operations, column 19, lines 49-50) and the decimal portion with the added correction value (e.g., error distributing means 907 for determining to which pixel the error data output from the error-to-be-distributed computing means 904 should be added, column 19, lines 59-62); a latch component (e.g., error distributing means 907, figure 25) that latches the decimal portion of the corrected image data to be connected to image data of a next pixel (e.g., error distributing means 907 for determining to which pixel the error data output from the error-to-be-distributed computing means 904 should be added, column 19, lines 59-62);

a quantization component (e.g., binarizing means block 903, figure 25) that receives an integral portion (upper bits) of the corrected image data and quantizes the received integer portion of the corrected image data (e.g., binarizing means 903 for binarizing a signal output from the data adding means 902, figure 25, column 19, lines 47-49); a buffer that stores the calculated quantization error (e.g., error distributing means 907 and block 908, figure 25) and an error diffusion component (e.g., error storing means block 908 and data adding means block 902, figures 25) that generates a correction value to be added to input data of a next pixel by diffusing the quantization error stored in said buffer (e.g., data adding means (block 902) for adding an input image signal to an error distributed from neighboring pixels, figure 25, column 19, lines 40-65).

Katayama does not explicitly disclose an inverse quantizing component that inverse-quantizes the quantized integer portion of the corrected image data, and outputs an inverse-quantized data; a calculation component that outputs a quantization error based on a difference between the integer portion of the corrected image data and the inverse-quantized data.

Ishikawa's 075 discloses an inverse quantizing component (e.g., inverse quantizer 31, figure 3) that inverse-quantizes the quantized integer portion of the corrected image data (e.g., output from quantizer 13 (integer portion), figure 3), and outputs an inverse-quantized data (e.g., the quantized representative values of the CMY signals outputted by the inverse quantizer 31, column 8, lines 19-21); a calculation component (e.g., The adder/subtractor 32, column 8, line 18) that outputs a quantization error based on a difference between the integer portion of the corrected image data

(e.g., subtracting the CMY signals outputted by the offset adder 17, column 8, lines 18-19) and the inverse-quantized data (e.g., the quantized representative values of the CMY signals outputted by the inverse quantizer 31, column 8, lines 19-21).

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to have modified Katayama to include an inverse quantizing component that inverse-quantizes the quantized integer portion of the corrected image data, and outputs an inverse-quantized data; a calculation component that outputs a quantization error based on a difference between the integer portion of the corrected image data and the inverse-quantized data as taught by Ishikawa's 075. It would have been obvious to one of ordinary skill in the art at the time of the invention to have modified Katayama by the teaching of Ishikawa to conveniently diffuse error to neighboring pixels to have better image quality.

With regard to claim 3, Katayama discloses further comprising a stop component that stops propagating the correction value in a case in which it is inappropriate to propagate the correction value to next and subsequent pixels (e.g., the error distribution controlling circuit, figures 6, column 7, line 61 – column 8, lines 63).

With regard to claim 7, Katayama discloses further comprising a numerical value limit component that limits the quantization error calculated by calculation component to a numerical value within a predetermined range (e.g., the error distribution controlling circuit, column 7, line 61 – column 8, line 65).

Referring to claim 20:

Claim 20 is the method claim corresponding to operation of the device in claim 1 with method steps corresponding directly to the function of device elements in claim 1. Therefore claim 20 is rejected as set forth above for claim 1.

Referring to claim 22:

Claim 22 is the method claim corresponding to operation of the device in claim 3 with method steps corresponding directly to the function of device elements in claim 3. Therefore claim 22 is rejected as set forth above for claim 3.

Referring to claim 26:

Claim 26 is the method claim corresponding to operation of the device in claim 7 with method steps corresponding directly to the function of device elements in claim 7. Therefore claim 26 is rejected as set forth above for claim 7.

Referring to claim 39:

Claim 39 is the computer-executable storage medium claim corresponding to operation of the device in claim 1 with instruction steps corresponding directly to the function of device elements in claim 1. Therefore claim 39 is rejected as set forth above for claim 1.

Claims 4-6, and 23-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Katayama et al. (Katayama) (US 5,488,673) and Ishikawa (US 6,330,075) as applied to claims 1 and 3 above, and further in view of Nakano et al. (Nakano) (US 6,977,756).

With regard to claim 4, Katayama and Ishikawa's 075 differ from claim 4, in that they do not explicitly show a clear component to clear data/error portion in latch/temporary memory in case in which it is inappropriate.

Nakano discloses a clear component to clear data/error portion in latch/temporary memory (e.g., it clears a content of the error holding register, column 5, lines 58-61).

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to have modified Katayama and Ishikawa's 075 to include a clear component to clear data/error portion in latch/temporary memory in case in which it is inappropriate conditions as taught by Nakano. It would have been obvious to one of ordinary skill in the art at the time of the invention to have modified Katayama and Ishikawa's 075 by the teaching of Nakano to clear data/error as needed.

With regard to claim 5, Nakano discloses further comprising a processing limit component that limits clearing by clear component when a scanning direction of the input image is reversed (e.g., adder 9 detects forward and reversed direction, column 9, lines 13-34).

With regard to claim 6, Nakano discloses wherein the case in which it is inappropriate to propagate the correction value to next and subsequent pixels includes at least one of a case in which a pixel of interest is a start pixel of a line, a case in which the pixel of interest has a value equal to a lower limit level of the input image, and a case in which the pixel of interest has a value equal to an upper limit level of the input image (column 8, line 48 – column 9, line 3).

Referring to claim 23:

Claim 23 is the method claim corresponding to operation of the device in claim 4 with method steps corresponding directly to the function of device elements in claim 4. Therefore claim 23 is rejected as set forth above for claim 4.

Referring to claim 24:

Claim 24 is the method claim corresponding to operation of the device in claim 5 with method steps corresponding directly to the function of device elements in claim 5. Therefore claim 24 is rejected as set forth above for claim 5.

Referring to claim 25:

Claim 25 is the method claim corresponding to operation of the device in claim 6 with method steps corresponding directly to the function of device elements in claim 6. Therefore claim 25 is rejected as set forth above for claim 6.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quang N. Vo whose telephone number is (571)270-1121. The examiner can normally be reached on 7:30AM-5:00PM Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David K. Moore can be reached on (571)272-7437. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Q. N. V./
Examiner, Art Unit 2625

/David K Moore/
Supervisory Patent Examiner, Art Unit 2625